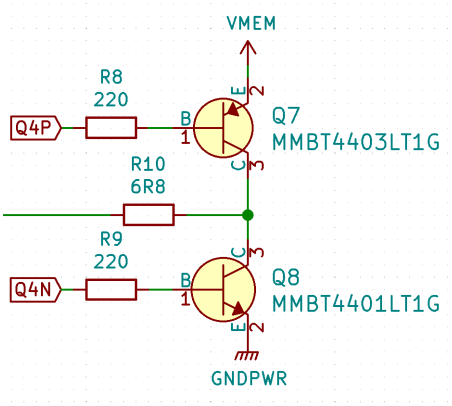
Code-Read and Write Cores

Core 64: Interactive Core Memory Badge, Andrew Geppert, 2019-08-24

Set – top end of the column wire and left end of row wire are positive (VMEM). Other ends negative (GNDPWR).
Clear - top end of the column wire and left end of row wire are negative (GNDPWR). Other ends positive (VMEM).

Each end of a single row or column wire can be connected to either VMEM (3-4V) or GNDPWR (0V). That means that two transistors must be enabled for a row or column wire to be energized. Since a core is set or cleared by the current from TWO wires, a total of 4 transistors must be enabled .



4403 PNP – Enabled with base LOW, or negative.
High side (sourcing) odd numbered matrix drive pins (7) with P suffix (Q4P). The load is connected to negative and the PNP transistor switches the positive voltage.

4401 NPN – Enabled with base HIGH, positive.
Low side (sinking) even numbered matrix pins (8) with N suffix (Q4N). The load is connected to positive and the NPN transistor switches the negative (low) side.

Safe state, all transistors inactive:

Enable Pin = LOW
Matrix Drive 1, 3, 5, 7, 9, 11, 13, 15, 17, 19 = HIGH
Matrix Drive 2, 4, 6, 8, 10, 12, 14, 16, 18, 20 = LOW

1. Since the output lines used to address the matrix may have other functions (like 17 is shared with the onboard Teensy LC LED), need to check all of the lines to see if any are not in the safe state for addressing the matrix.
   1.1. If a line is set other than safe [future work]
   1.2. save the state for later reference [future work]
   1.3. set all matrix lines and the enable line to safe states.
2. Set a core to 1 (bit 0, upper left corner)
   2.1. Set column (X0)
      2.1.1. Connect top end of column (XT0) to VMEM
         2.1.1.1. Activate top transistor (Q3P), Pin_Matrix_Drive_5, LOW
      2.1.2. Connect bottom end of column (XB0) to GNDPWR
         2.1.2.1. Activate bottom transistor (Q1N), Pin_Matrix_Drive_2, HIGH
   2.2. Set row (Y0)
      2.2.1. Connect left end of row (YL0) to VMEM
         2.2.1.1. Activate left transistor (Q7P), Pin_Matrix_Drive_13, LOW
      2.2.2. Connect right end of row (YR0=YR4=YL4=YL6) to GNDPWR

2.2.2.1. Activate right transistor (Q9N), Pin_Matrix_Drive_17, HIGH

2.3. Set Enable
  2.3.1. HIGH
  2.3.2. Wait ?? ns to lock in the magnetized state.
  2.3.3. Clear enable
2.4. Return 4 transistors to safe states
2.5. Return any other shared lines that weren't initially safe, to the state they were at.
2.6. End

3. Clear a core to 0 (bit 0, upper left corner)

Decode bit position (0…63) to matrix drive transistors (1…20)
Each row of this array corresponds to the bit #. First row is bit 0, last row is bit 63.
Row contains four matrix drive #s, each followed by the corresponding low/high needed to activated the transistor.
Odd numbered drive line transistors are active LOW
Even numbered drive line transistors are active HIGH

```
uint8_t CoreMemoryMatrixDriveSetBitTransistors[] = {
  { 5,0,2,1, 13,0,17,1},
…
  { }
};
```

Store core value as:

```
uint64_t CoreMemorySixtyFourBit = 0b0000…1111;
```

-AND-

```
bool CoreMemoryArray[] = {
  { 0, 1, 2, 3, 4, 5, 6, 7, 8},
…
  {55,56,57,58,59,60,61,62,63}
};
```

Core Library Basics

1. CoreWriteBit (position #, value)
   1.1. Position # is 0 to 63 for the 64 bits. Starting upper left as 0, left to right, top to bottom, ending with bit 63 in the lower right.
   1.2. Value is Boolean 0 or 1
   1.3. Returns nothing
2. CoreReadBit (position #)
   2.1. Returns value Boolean 0 or 1
3. CoreWriteByte (position #, value)
   3.1. Position # is 0 for the top row, 7 for bottom row. MSb is left.

    3.2. Value is uint8_t 0-255
    3.3. Returns nothing
4. CoreReadByte (position#)
    4.1. See above
5. CoreWrite64bits (value)
    5.1. Value is uint64_t
    5.2. Returns nothing
6. CoreRead64bits (void)
    6.1. Return uint64_t